REMARKS

Claims 3-10 and 21-35 are pending in the present application. Claims 21 and 22 have been amended. Claims 23-35 have been presented herewith.

Priority Under 35 U.S.C. 119

Applicant notes the Examiner's acknowledgment of the Claim for Priority under 35 U.S.C. 119, and receipt of the certified copy of the Priority Document in parent application Serial No. 10/283,189.

Information Disclosure Statement

Enclosed are copies of an Information Disclosure Statement and two (2) PTO/SB/08A Forms filed on June 2, 2005. Also enclosed is a copy of dated, stamped postcard receipt provided as evidence that the above noted Information Disclosure Statement was received by the U.S. Patent Office. **The Examiner is respectfully requested to acknowledge receipt of the above noted Information Disclosure Statement, and to confirm that the corresponding references have been considered and will be cited of record in the present application**.

Drawings

The drawings have been objected, whereby the Examiner has required that Figs. 1 – 5 be designated as "PRIOR ART". Accordingly, enclosed are three (3) drawing

Annotated Sheets, wherein Figs. 1 – 5 have been denoted as "PRIOR ART". Also enclosed are three (3) drawing Replacement Sheets, incorporating the above noted corrections. **The Examiner is respectfully requested to acknowledge receipt and acceptance of the drawing Replacement Sheets.**

Claim Rejections-35 U.S.C. 103

Claims 3-10, 21 and 22 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Itonaga reference (U.S. Patent Application Publication No. 2002/0061639) in view of the Yu et al. reference (U.S. Patent Application Publication No. 2003/0029715). This rejection, insofar as it may pertain to the presently pending claims, is traversed for the following reasons.

The method for fabricating a semiconductor device of claim 21 includes in combination "forming a metallic layer on the silicon region of the heated substrate by a straight sputtering method so as to sputter straightly to the silicon region, wherein the metallic layer has a first thickness"; "forming a protective layer on the metallic layer, wherein the protective layer protects the metallic layer from surrounding atmosphere and wherein the protective layer has a second thickness greater than the first thickness"; "forming a metallic silicide layer in an interface between the silicon region and the metallic layer under the protective layer by a first heat treatment, so that the metallic silicide layer has a high resistance crystalline structure"; "removing the protective layer"; and "subjecting the metallic silicide layer to a second heat treatment

after said removing the protective layer, so that the metallic silicide layer has a low resistance crystalline structure".

The Examiner has primarily relied upon the Itonaga reference as disclosing all the features of claim 21, except for sputtering the metallic layer onto the substrate by a straight sputtering method, so as to sputter straightly to the silicon region.

However, as described in paragraph [0071] of the Itonaga reference with respect to Fig. 1C, formation of a metallic silicide layer 10a under protective layer 9 between silicon layer 7 and metal layer 8 is by a first rapid thermal anneal (RTA). The protective layer 9 and the unreacted metal film 8a are then removed, as described in paragraph [0073] and as shown in Fig. 2A. Thereafter, arsenic ions are implanted into metal silicide film 10a "so as to turn the polysilicon or silicon into an amorphous state", as described in paragraph [0074] with respect to Fig. 2B. As described in paragraph [0076] of the Itonaga reference with respect to Fig. 2C, the structure is then subjected to a second RTA so as to convert the amorphous metal silicide film 10b into a structurally-stable silicide layer 10c.

Applicant respectfully submits that the process as disclosed in the Itonaga reference is different from the method of fabricating a semiconductor device of claim 21, because the process in the Itonaga reference requires formation of an amorphous silicide layer prior to the second RTA. The process of the Itonaga reference thus requires additional steps which increase complexity and expense. Applicant therefore respectfully submits that the method of fabricating a semiconductor device of claim 21

would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection, insofar as it may pertain to claims 3-10, 21 and 22, is improper for at least these reasons.

Claims 23-35

The method of manufacturing a semiconductor device of claim 23 includes in combination "forming a metallic layer on the silicon region of the heated substrate by a straight sputtering method"; "forming a protective layer on the metallic layer"; "forming a first metallic silicide layer on the silicon region under the protective layer by a first heat treatment, the first metallic silicide layer having a high resistance crystalline structure"; "removing the protective layer"; and "subjecting the first metallic silicide layer to a second heat treatment after said removing the protective layer, so as to change the first metallic silicide layer into a second metallic silicide layer having a low resistance crystalline structure".

Applicant respectfully submits that the method of manufacturing a semiconductor device of claim 23 would not have been obvious in view of the prior art as relied upon by the Examiner for at least somewhat similar reasons as set forth above with respect to claim 21. Particularly, the process in the Itonaga reference is different than the method of claim 23, because the process in the Itonaga reference requires formation of the amorphous silicide layer prior to the second RTA. Applicant therefore respectfully submits that this rejection, insofar as it may pertain to claims 23-29 is improper for at

least these reasons.

The method of manufacturing a semiconductor device of claim 30 includes in combination "forming a metallic layer on the silicon region of the heated substrate by a straight sputtering method"; "forming a protective layer on the metallic layer"; "forming a high resistance metallic silicide layer on the silicon region under the protective layer by a first heat treatment, the high resistance metallic silicide layer having a first crystalline structure"; "removing the protective layer"; and "subjecting the high resistance metallic silicide layer to a second heat treatment after said removing the protective layer, so as to change the high resistance metallic silicide layer into a low resistance metallic silicide layer having a second crystalline structure".

Applicant respectfully submits that the method of manufacturing a semiconductor device of claim 30 would not have been obvious in view of the prior art as relied upon by the Examiner for at least somewhat similar reasons as set forth above with respect to claim 21. Particularly, the process in the Itonaga reference is different than the method of claim 30, because the process in the Itonaga reference requires formation of the amorphous silicide layer prior to the second RTA. Applicant therefore respectfully submits that this rejection, insofar as it may pertain to claims 30-35 is improper for at least these reasons.

Conclusion

The Examiner is respectfully requested to reconsider and withdraw the corresponding rejection, and to pass the claims of the present application to issue, for at least the above reasons.

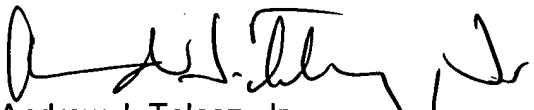
In the event that there are any outstanding matters remaining in the present application, please contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (571) 283-0720 in the Washington, D.C. area, to discuss these matters.

Pursuant to the provisions of 37 C.F.R. 1.17 and 1.136(a), the Applicant hereby petitions for an extension of one (1) month to September 18, 2005, for the period in which to file a response to the outstanding Office Action. The required fee of $120.00 should be charged to Deposit Account No. 50-0238.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment for any additional fees that may be required, or credit any overpayment, to Deposit Account No. 50-0238.

Respectfully submitted,

VOLENTINE FRANCOS & WHITT, P.L.L.C.



Andrew J. Telesz, Jr.
Registration No. 33,581

One Freedom Square
11951 Freedom Drive, Suite 1260
Reston, Virginia 20190
Telephone No.: (571) 283-0270
Facsimile No.: (571) 283-0740

Enclosures:
- Copies of Information Disclosure Statement and PTO/SB/08A Forms filed June 2, 2005
- Copy of dated, stamped postcard receipt
- Three (3) drawing Annotated Sheets
- Three (3) drawing Replacement Sheets

FIG.1
PRIOR ART

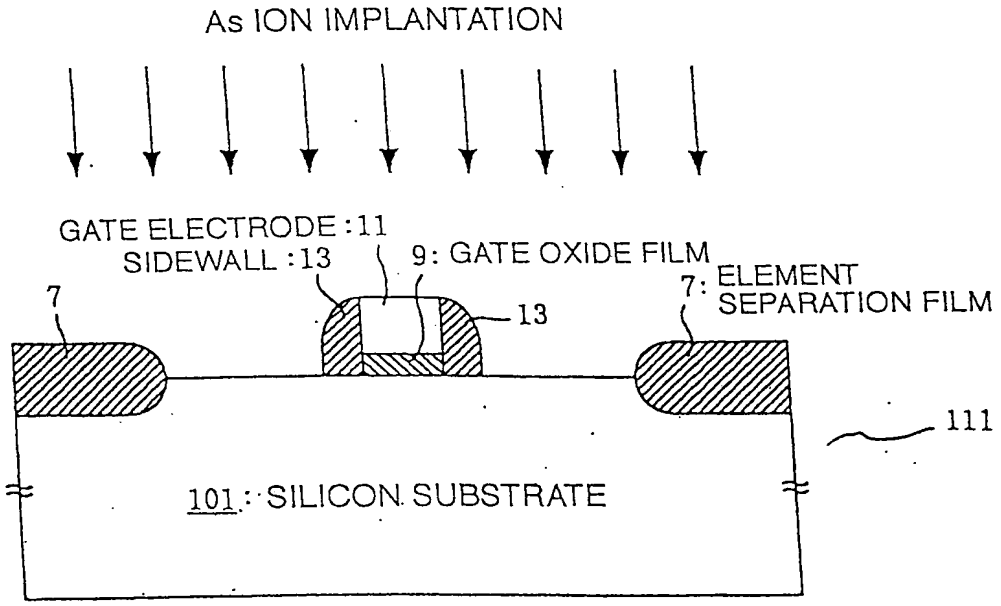


FIG.2
PRIOR ART

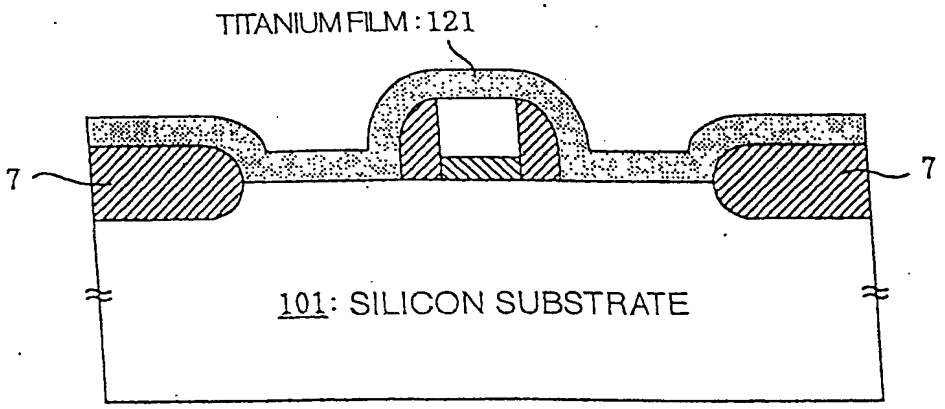


FIG. 3
PRIOR ART

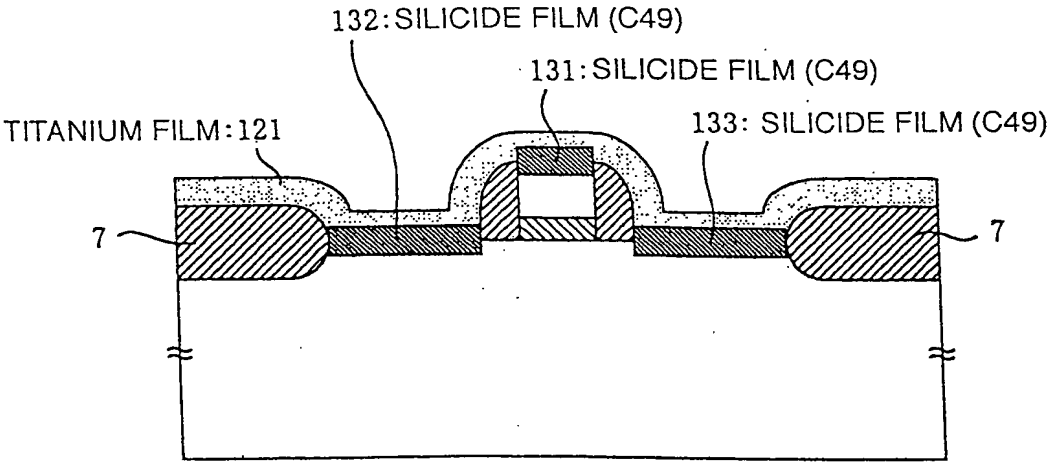


FIG. 4
PRIOR ART

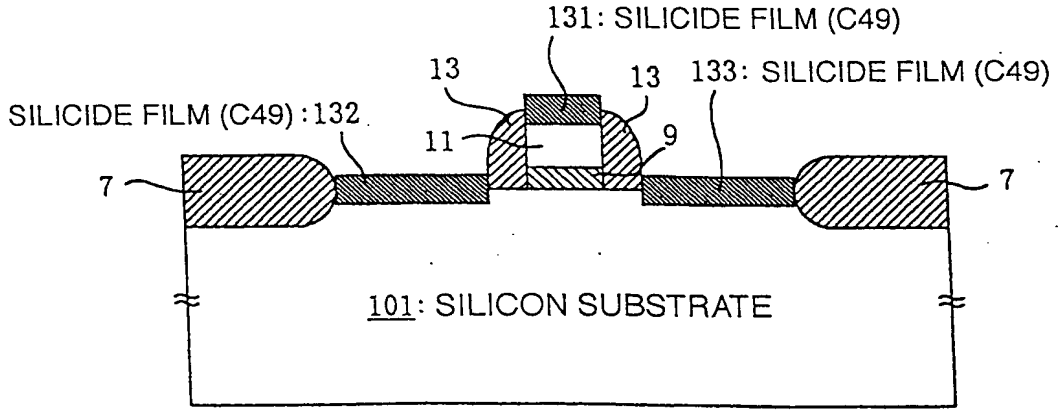


FIG. 5

PRIOR ART

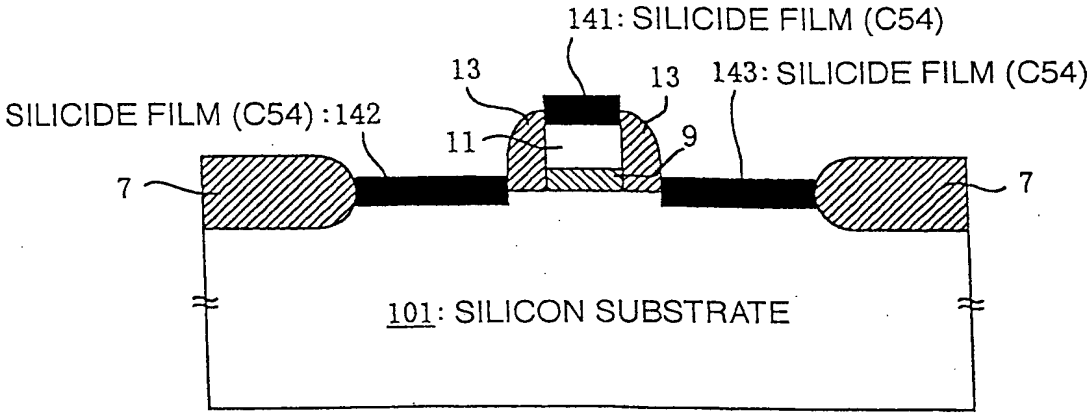


FIG. 6